Partial translation of Japanese Patent Application Laid-open 11-121731

[0051] [Embodiment 2] This embodiment is a modified example of the matrix circuit of Embodiment 1. Fig. 7 is an equivalent circuit diagram of 2×2 pixels of an image sensor of this embodiment. Fig. 8 is a schematic plan view of the matrix circuit of this embodiment. This embodiment is different from Embodiment 1 in that the selection transistor Ts is configured as so called a multi-gate structure having two gate electrodes. In Figs. 7 and 8, the same reference symbols as Figs. 1 and 4 designate the same constituents.
[0052] As shown in Fig. 8, two gate electrodes 301 and 302 of the selection transistor Ts are integrally formed in the selection line 101. Further, similar to Embodiment 1, active layers of all thin film transistors formed in a unit section 300 is formed in one island area 303. A photoelectric converter (photodiode PD) may be formed similar to Embodiment 1, and in Fig. 8, a rectangular area 304 shown by a heavy line represents a plane pattern of a lower electrode.
[0053] This embodiment attempts to reduce a leakage current of the selection transistor Ts during non-selection by configuring the selection transistor Ts to have a structure in which two transistors are connected in series. If a current leaks from the selection transistor Ts during non-selection, a signal current output from a signal line is reduced. Further, the leakage current becomes a noise with

respect to a signal current output from other pixels. This embodiment solves these two problems by configuring the selection transistor Ts as a multi-gate type.

[0054] In this embodiment, since two gate electrodes 301 and 302 of the selection transistor Ts are formed in the selection line 101, a pixel pitch in a horizontal direction becomes 13a (a is a design rule) and becomes larger than that of Embodiment 1, but since the power line 104 is shared in two adjacent columns, the pixel pitch is more shortened than the conventional pixel pitch 15a.

[0055] [Embodiment 3] This embodiment is a modified example of the matrix circuit of Embodiment 1. Fig. 9 is an equivalent circuit diagram of 2×2 pixels of an image sensor of this embodiment. Fig. 10 is a schematic plan view of the matrix circuit of this embodiment. This embodiment is different from Embodiment 1 in that the reset transistor Tr is configured as a so called multi-gate structure having two gate electrodes. In Figs. 9 and 10, the same reference symbols as Figs. 1 and 4 designate the same constituents. A photoelectric converter (photodiode PD) may be formed similar to Embodiment 1, and in Fig. 10, a rectangular area 314 shown by a heavy line represents an area in which a lower electrode is formed.

[0056] As shown in Fig. 10, two gate electrodes 311 and 312 of the reset transistor Tr are integrally formed in the selection line 102. Further, similar to Embodiment 1, active layers constituting all thin film transistors formed in a

unit section 310 is formed in one island area 313. Further, in this embodiment, a pixel pitch in a horizontal direction becomes 12a (a is a design rule) and becomes larger than that of Embodiment 1, but since the power line 104 is shared in two adjacent columns, the pixel pitch can be more shortened than the conventional pixel pitch 15a.

[0057] This embodiment attempts to reduce a leakage current of the reset transistor Tr during non-selection by configuring the reset transistor Tr to have a structure in which two transistors are connected in series. If a current leaks from the reset transistor Tr during non-selection, a potential of the gate electrode 206 of the amplification transistor Ta which is in a floating state at this time rises. A magnitude of a current amplified by the amplification transistor Ta corresponds to a reduction amount of the potential of the gate electrode. Therefore, if the potential of the gate electrode rises, a drain current output from the amplification transistor Ta is reduced. A signal current read out from the pixel becomes small. As a result, a resolution deteriorates and unevenness in brightness of an image occurs. This embodiment reduces the leakage current to solve this problem by configuring the reset transistor Tr as a multi-gate type.

[0058] [Embodiment 4] This embodiment is a modified example of the matrix circuit of Embodiment 1. Fig. 11 is an equivalent circuit diagram of 2×2 pixels of an image sensor of this embodiment. Fig. 12 is a schematic plan view of the

matrix circuit of this embodiment. This embodiment is different from Embodiment 1 in that the selection transistor Ts and the reset transistor Tr are each configured as a so called multi-gate structure having two gate electrodes. In Figs. 11 and 12, the same reference symbols as Figs. 1 and 4 designate the same constituents.

[0059] Two gate electrodes 321 and 322 of the selection transistor Ts are integrally formed in the selection line 101, and two gate electrodes 323 and 324 of the reset transistor Tr are integrally formed in the reset line 102. Further, active layers of six thin film transistors disposed in a unit section 320 is configured in one island area 325. A photoelectric converter (photodiode PD) may be formed similar to Embodiment 1, and in Fig. 12, a rectangular area 326 shown by a heavy line represents a plane pattern of a lower electrode.

[0060] This embodiment can simultaneously solve the problems caused by the leakage currents of the selection transistor Ts and the reset transistor Tr as illustrated in Embodiment 2 and Embodiment 3 by configuring the selection transistor Ts and the reset transistor Tr to have a double-gate structure. Further, in this embodiment, a pixel pitch in a horizontal direction is 13a (a is a design rule) which is the same as Embodiment 2.

[0061] In Embodiment 1 to 4 described above, although the image sensor formed on an insulating surface has been explained, it is apparent that an effect of shortening a

pixel pitch can be obtained even when the image sensor is formed in a single crystal silicon substrate by employing the plan structure of the element according to the present invention.

[Fig. 7]

101: SELECTION LINE

102: RESET LINE

103: SIGNAL LINE

103: SIGNAL LINE

104: POWER LINE

300: UNIT SECTION

[Fig. 8]

300: UNIT SECTION

301, 302: GATE ELECTRODE OF Ts

303: ISLAND AREA

[Fig. 9]

101: SELECTION LINE

102: RESET LINE

103: SIGNAL LINE

103: SIGNAL LINE

104: POWER LINE

310: UNIT SECTION

[Fig. 10]

310: UNIT SECTION

311, 312: GATE ELECTRODE OF Tr

313: ISLAND AREA

[Fig. 11]

101: SELECTION LINE

102: RESET LINE

103: SIGNAL LINE

103: SIGNAL LINE

104: POWER LINE

320: UNIT SECTION

[Fig. 12]

320: UNIT SECTION

321, 322: GATE ELECTRODE OF Ts

323, 324: GATE ELECTRODE OF Tr

325: ISLAND AREA